This 2-day workshop is the first event organized by the ECSI Interest Group on UML for Embedded Systems. The workshop is intended to give an overview of the current status of the development and application of system-level modeling methods and techniques based upon UML for embedded systems and Systems-on-Chip. The workshop is a forum to exchange knowledge and experiences, and updates on the evolving standardization process and supporting methods. The objective of the ECSI Interest Group is to support and advance system modeling and model-driven engineering for Embedded Systems and Systems-on-Chip design. It joins researchers and suppliers of methods and tools with practitioners and embedded system designers from a broad range of application domains. Modeling is the main engineering activity and promoting a model-driven approach from concept to realization. By making available the information from the diversity of activities and initiatives in this area, the Interest Group aims to support in the concertation and coordination of them from the perspective of Embedded Systems and Systems-on-Chip leading to a wide-spread use and effective standardization.

While UML was designed as a system-level visual language to analyze, specify, design, verify and validate software-intensive systems, UML is not restricted to modeling software. UML has its strengths at higher, more architectural levels, and it has gained attention for the development of complex embedded systems and heterogeneous SoCs.

UML profiles are the means to provide user-defined extensions, notations and terminologies, and to support application domain specific engineering methods. This workshop presents and discusses the status and application of such profiles addressing the specific needs and characteristics of embedded systems engineering, real-time hardware/software systems and heterogeneous Systems-on-Chip.

In the first session a tutorial will be presented to introduce the expectations behind the application of UML in embedded system design. It will discuss the motivation of why different profiles are needed and what the relations are between them and to other profiles. It will present model-driven architecture (MDA) and design and position the profiles in the context of levels of application and focus in system design flow from requirements, analysis to implementation and verification. The tutorial will also give an outline of the standardization activities and take-up.

This session is followed by detailed presentations on main profiles that are being standardized for embedded systems and Systems-on-Chip design. The Systems Modeling Language (SysML) is the result of a joint initiative of the Object Management group (OMG) and the International Council on Systems Engineering (INCOSE) to provide a general purpose modeling language for Systems Engineering (SE), based on UML. MARTE is a UML profile voted at OMG for the modeling and analysis of real-time embedded systems. It covers both hardware and software aspects and addresses temporal and synchronization modeling, quality-of-service, schedulability and performance analysis. UML for SoC is a profile designed to describe System-On-Chip specific information using UML covering abstraction levels from transactional level modeling to register transfer level. UML for SystemC is a UML 2.0 profile of the SystemC language for use in UML structural and behavioral diagrams to model the functionality expressed by processes and channels in a SystemC specification.

The third session will investigate in more detail the relations between the different profiles such as MARTE and UML for SoC. In particular, it will provide an overview of models of computation, address the representation of platforms and architectures, and present a UML 2.0 profile based on IP-block granularity and libraries for platform components. The following sessions will provide the industry point of view on their needs and experiences with system engineering methods and modeling techniques. A demonstration of a full featured WLAN terminal implementation will be given starting from a behavior entirely specified in UML2.0. The terminal executes on an FPGA including multiple processors, IP-blocks and real-time execution monitor.
EDA tool vendors will present their support for UML based embedded system design, such as model-driven architecture design environment to predict behavior and performance through system-level modeling and simulation, a UML subset that is fully executable and translatable, and an environment to create own UML profiles specified in XML.

As a workshop, the event will give the participants ample opportunities for discussions and interactions to exchange experiences and influence the ongoing standardization activities.
SysML - Wolfgang Mueller, C-Lab

SysML is an extension to UML which allows modeling a system from a Systems Engineering (SE) point of view. Strong similarities exist between the methods used in the area of SE and complex embedded system design, such as the need for precise requirements management, heterogeneous system specification and simulation, system validation and verification. This paper presents the main features of SysML and identifies the opportunities it provides improve UML-based development processes for embedded systems.

The Systems Modeling Language (SysML) is the result of a joint initiative of OMG and the International Council on Systems Engineering (INCOSE). The aim is to provide a general purpose modeling language for Systems Engineering (SE), based on UML. This field covers complex systems which include a broad range of heterogeneous domains, in particular, hardware and software.

INCOSE selected UML as a result of the increasing usage and acceptance of UML among the Systems Engineering community, and the benefits of extending UML as a standard systems modeling language:

- UML is a robust language. UML is supported by an extensive infrastructure of tool vendors and training that the Systems Engineering community can leverage.
- UML has built-in refinement mechanisms. A UML extension for SE would facilitate integration with software UML models and on-going efforts towards hardware UML models.
- A defined technology adoption process and broad user representation are supported by the OMG, which assist in further evolution of the language.
- UML is supported by an extensive infrastructure of tool vendors and training that the Systems Engineering community can leverage.

Strong similarities exist between the methods used in the area of Systems Engineering and embedded system design, such as the need for accurate requirements elicitation, heterogeneous system specification and simulation, and system validation and verification. Several features from SysML can therefore be applied to embedded system design.

MARTE – Laurent Rioux, Thales

(with inputs from Thales, Artisan SW, CEA, Telelogic/I-logix, INRIA, Mentor Graphics, Cofluent, Barco, Nokia, Tampere University of Technology)

The MARTE proposal addresses the set of general requirements:

- Proposals shall support modeling and analysis of RTES including its SW and abstract HW aspects.
- SW and HW profile parts can be reusable independently.
- Based on the version of the UML 2 metamodel and notation.
- Align as much as possible with the Quality-of-Service (QoS) and Fault-Tolerance (FT) profile.
- Meta-models normative as a basis for tool integration.
- Any proposed extensions to UML that impact the UML metamodel shall be expressed in a way that ensures that the UML metamodel remains a MOF compliant metamodel.
- Address the issues deferred in the RTF report for the UML Profile Schedulability, Performance and Time (SPT) v1.1.
- Provide means to ease reuse of SPT-v1.1 based models

The specific requirements that MARTE addresses are organized in three groups:

- Time and concurrent resources (temporal models, measures of time and performance, synchronization, heterogeneous platforms, high-level modeling constructs)
- Real-time and embedded modeling (static resource allocation, specific QoS, behavioral and structural requirements: e.g. allocation capabilities of SW to abstract HW, component-based architecture modeling)
- Scheduling, performance analysis (schedulability and performance meta-models, annotations, timed-utility functions)
The UML for SoC profile is targeted and designed to describe the SoC (System On Chip) specific information. The expected advantages of using this profile are to add the SoC description capability to UML by providing the following representation capabilities:

- hierarchical representation of modules and channels, which are fundamental to SoC designs
- role of modules and information transferred between them using only one diagram

The proposed UML for SoC concepts are very close to SystemC and allow automatic SystemC code generation. The covered abstraction levels are:

- from transactional level modeling (TLM)
- to register transfer level (RTL)

The UML for SoC profile mainly uses the UML 2.0 structure diagrams. It proposes the stereotypes that allow the structural modeling, communication modeling, operation and property modeling. The defined stereotypes are:

- module
- channel (clock channel, reset channel)
- protocol interface
- port
- connector
- SoC data type
- process
- protocol
- data
- controller

UML for SystemC is a UML 2.0 profile of the SystemC language that reflects the core layer (or layer 0), and the layer 1 (where a predefined set of channels, ports and interfaces are defined) of SystemC. The profile specifies the stereotypes that can be used in various UML structural diagrams (like class diagrams and composite structure diagrams) for representing the structural building blocks and stereotypes that can be used in various UML behavioral diagrams (such as UML method state machines) for modeling the functionality expressed by processes and channels in a given SystemC specification.

The main target of this UML profile is to provide a means for hardware and software engineers to improve the current industrial SoC (System-on-Chip) design flow joining the capabilities of UML and SystemC to operate at system-level. Since the profile provides a straightforward translation to SystemC code, a SystemC code generator has been developed that generates SystemC code from the UML models for both structural and behavioral aspects. The code generator follows the Model Driven Approach: C/C++/SystemC is adopted as action languages at PSM (Platform Specific Model) level, generating code for the full model, even when no action language is adopted at PIM (Platform Independent Model) level. In practice the UML profile for SystemC allows to embed parts of the PSM in the PIM.

The TUT-Profile is a well-defined UML2.0 profile for large embedded systems design. The profile defines a set of UML stereotypes that extend the UML2.0 metamodel with standard extension mechanisms. Thus the TUT-Profile is compatible with commercial UML2.0 tools. TUT-Profile is based on IP-block granularity and libraries for platform components. The new feature is to keep all essential design information explicitly at UML2.0 level without any auxiliary languages, models or descriptions.

The TUT-Profile divides system modeling into the design of application, architecture and mapping models. The models also contain non-functional constraints for specification, design automation, analysis and implementation. The models also include back-annotated performance values from real implementation or simulation.

The profile is supported by the KOSKI a design framework that transforms UML2.0 specifications to Multi-Processor SoC implementations. It includes automated steps for program code generation, heterogeneous IP-block architecture exploration, application distribution among processors with RTOS integration and MP-SoC platform assembly. From the implementation real-time performance and memory measurements are back-annotation to the UML2.0 models for constraints matching.

The design flow is entirely governed by UML2.0 models with TUT-Profile. UML2.0 models and library components are used as such without separate manual programming or conversions.
ECSI Institute Workshop:  
UML Profiles for Embedded Systems

Advance Programme

Place: Hotel Brébant (in downtown), Paris, France  
Date: March 27-28, 2006 – 2 days event

Day 1

Session 1: Introduction (Gjalt de Jong, ECSI)
- welcome and introduction ECSI interest group on UML for Embedded Systems  
- the expectations behind the application of UML in Embedded System design  
- overall picture: why different profiles are proposed, what are the relations between them  
- relations to other profiles  
- the levels of application, focus in design flows  
- standardization activities

Session 2: UML Profiles Presentation (1.5-2h each)
- SysML (Wolfgang Mueller, C-Lab)  
  o The Systems Modeling Language (SysML) is the result of a joint initiative of OMG and the International Council on Systems Engineering (INCOSE) to provide a general purpose modeling language for Systems Engineering (SE), based on UML.

- MARTE (Laurent Rioux, Thales)  
  o A UML profile voted at OMG for the modeling and analysis of real-time embedded systems. It covers both hardware and software aspects and addresses temporal and synchronization modeling, quality-of-service, schedulability and performance analysis.

- UML for SoC (Sreeranga P. Rajan, Fujitsu)  
  o A profile designed to describe System-On-Chip specific information using UML covering abstraction levels from transactional level modeling to register transfer level.

- UML for SystemC (Sara Bocchio, Alberto Rosti, ST & Elvinia Riccobene, U Milan, P Scandurra, U Catania)  
  o A UML 2.0 profile of the SystemC language for use in UML structural and behavioral diagrams to model the functionality expressed by processes and channels in a SystemC specification.

Panel: Q&A from audience (Moderator: Gjalt de Jong)
Day 2

Session 3: Relations between UML profiles and other hot topics

Presentations and discussions on:
- MARTE and UML for SoC - Architecture models and platform representations (Pierre Boulet, LIFL, France) : discussing the different needs addressed by these profiles and how they can be used together in a model driven methodology to design embedded systems.
- Models of Computation (Fernando Herrera, UCantarabria, Spain) : the detection of needs and issues to connect UML profiles with heterogenous specification methodologies used for implementation of embedded systems.
- Use of UML2.0 standard extension mechanism for component-based design flow compatible with commercial UML 2.0 tools (Tero Tangas, TUT, Finland)

Session 4: Industry Needs and Experiences

Requirements for and applications of UML based methods for embedded systems and SoCs presented from:
- Nokia (Tero Tangas, TUT) : demonstrating the Koski design flow by the implementation of full featured WLAN terminal implementation starting from a behavior entirely specified in UML2.0.
- Thales (TBD) : prototyped engineering solutions for distributed and heterogenous embedded systems
- ST Microelectronics (Alberto Rosti) : link between UML specification and SystemC TLM
- Airbus : the TOPCASED integrated development process from system specification to product architecture.

Session 5: EDA Tool Support

Introduction and overview of UML support for embedded systems and SoCs from:
- Mentor Graphics (Thomas Ulber) : Why Systems-on-Chip needs more UML like a Hole in the Head - Executable and Translatable UML (XtUML), a selected subset of UML to support the needs of execution- and translation based development for system partitioning, automatic hardware/software interface generation and system integration.
- CoFluent (Vincent Perrier) : Secure prediction of behavior and performance through system-level modeling and simulation from partial hardware and software using model-driven architecture design approaches for system architecting and timed-behavioral modeling.
- SparxSystems (Peter Lieber) : Enterprise Architect and the embedded world – A generic UML profile mechanism for loading and working with different profiles. UML profiles are specified in XML files allowing to create own profile to describe modelling scenarios peculiar to your development environment
- Artisan SW (Olivier Casse): a provider of UML modelling tools for modeling for real-time embedded systems modeling and software engineering, and provide support for SysML.

Session 6: Final Discussion

Forum to discuss experiences needs for standardization, and their effective use and deployment. Identification and definition of the next steps needed for UML for Embedded Systems and Systems-on-Chip.
HOTEL BREBANT

30-32, bd Poissonnière
75009 PARIS

Tel. : (+33) (0)1.47.70.25.55
Fax : (+33) (0)1.42.46.65.70
hotel.brebant@wanadoo.fr

Metro : Grands Boulevards
RER : Auber (Direct to Disneyland Paris)
Location : 500 m from to Opera, and Grands Boulevards.